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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,015	03/31/2004	Darren Slawecki	42P17273	9217

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EXAMINER	
NGUYEN, HAI L	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.D

Office Action Summary	Application No.	Applicant(s)	
	10/815,015	SLAWECKI, DARREN	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,14-18,21-29 and 32* is/are rejected.

7)☒ Claim(s) *8-13,19,20,30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *31 March 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: the claimed limitations are redundant. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are the structural and/or functional connections between the following elements: one of hardware behavioral code, register transfer level code, a netlist, a circuit layout, a clock enable circuit, a falling edge delay circuit, and a rising edge delay circuit.

4. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are the structural and/or functional connections between the following elements: a microprocessor, a clock distribution network, and a clock delay circuit.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 3-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Tang (US 6,859,082).

With regard to claims 1, Tang discloses in Figs. 3,4&9 a delay circuit, comprising a first circuit having a circuit input to receive a reference signal (314) and a circuit output to output a delayed signal (318); a falling edge delay circuit (340) coupled to the first circuit to control delay of a falling edge of the reference signal; and a rising edge delay circuit (350) coupled to the first circuit to control delay of a rising edge of the reference signal.

With regard to claim 3 and 5-7, the reference also meets the recited limitations in these claims.

With regard to claim 4, the reference also meets the recited limitations in the claim (see column 6, lines 4-11; and Fig. 9).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang in view of Lee (US Pat. 6,462,597).

With regard to claim 2, the above discussed circuit of Tang meets all of the claimed limitations except for an enable circuit further including an enable input to enable the delay circuit. Lee teaches in Fig. 3 a circuit including an enable circuit (G1) for allowing the circuit to be disabled when the circuit is not in use. Therefore, it would have been obvious to one skilled in the art at the time of applicant's invention was made to implement the enable circuit in the delay circuit of the reference (Figs. 3,4&9 of Tang) in order to conserve power by disabling when the delay circuit is not in use.

Claim 14 is similarly rejected; note the above discussion with regard to claims 1 and 2.

Claim 15 is similarly rejected; note the above discussion with regard to claim 4.

With regard to claims 16-18, the reference also meets the recited limitations in these claims.

9. Claims 22-27, 29, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kliza et al. (US Pat. 5,852,640) in view of the admitted prior art (APA), Fig. 1 in the present application, and Tang.

With respect to claim 22, Kliza et al. in Fig. 5 shows a circuit comprising a clock distribution network to distribute a reference clock signal (35) throughout the circuit; clock delay circuits (36-39); and a pluralities of digital subsystems (41-44), it is well known in the art that a digital subsystem may be constituted by any types of digital circuits including latches and logic

clusters as shown by the admitted prior art (APA), Fig. 1 in the present application. The references meet all the claimed limitations except for the structural limitations of the delay circuits are not as same as the structural limitations recited in the claim. Tang teaches in Figs. 3,4&9 a delay circuit having claimed limitations; note the above discussion with regard to claim 1. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to replace the clock delay circuits (36-39 in Fig. 5 of Kliza et al.) in the circuit of the prior art with the clock delay circuits as taught by Tang in order to selectively adjust the time delay of the clock delay circuits with the control signals.

With regard to claims 23, 24, 26, and 27, the references (Figs. 3,4&9 of Tang) also meet the recited limitations in these claims.

With regard to claim 25, the clock delay circuits are grouped into domains of the integrated circuit, the falling delay inputs and the rising delay inputs of the clock delay circuits coupled to receive the same falling delay signals and the same rising delay signals within each of the domains. Naturally, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to group clock delay circuits, which have same time delay characteristics, into domains of the integrated circuit, if there are several clock delay circuits needed for that part of the circuit. Then would be obvious to have the falling delay inputs and the rising delay inputs of the clock delay circuits coupled to receive the same falling delay signals and the same rising delay signals within each of the domains for not providing unnecessary extra wiring.

With regard to claims 29 and 32, the references (the APA, Fig. 1 in the present application) also meet the recited limitations in these claims.

Allowable Subject Matter

10. Claims 8-13, 19, 20, 30, and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a delay circuit (300 in instant Fig. 3), as recited in claims 8, 19, and 30, having specific structural limitations such as the enable circuit comprises a NAND logic gate (L1) having first and second NAND inputs and a NAND output, the first NAND input coupled to the clock input (320) and the second NAND input coupled to the enable input (325); a first pull up path including a first transistor (T1) to selectively couple the NAND output to the falling edge delay circuit (310); a pull down path including second and third transistors (T2, T3) coupled in series to selectively couple the NAND output to the rising edge delay circuit (315); and an inverter (L2) coupling the NAND output to the circuit output (330); and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a delay circuit (500 in instant Fig. 5), as recited in claim 11, having specific structural limitations such as the enable circuit comprises a NAND logic gate (L1) having first and second NAND inputs and a NAND output, the first NAND input coupled to the clock input (320) and the second NAND input coupled to the enable input (325); a first inverter (L10) coupling the clock input to the first NAND input; a pull up path including a first transistor (T1) to selectively couple the NAND output to the rising edge delay circuit (510); a pull down path including second and third transistors (T2, T3) coupled in series to selectively couple the NAND output to the falling edge delay circuit (515);

and an second inverter (L2) coupling the NAND output to the circuit output (330); and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Salcedo et al. (US 6,424,197) is cited as of interest because it discloses a rising and falling edge aperture delay control circuit in analog front end of imaging system.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

1. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
June 11, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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